EE 3714 Test #4 Solutions Fall 99

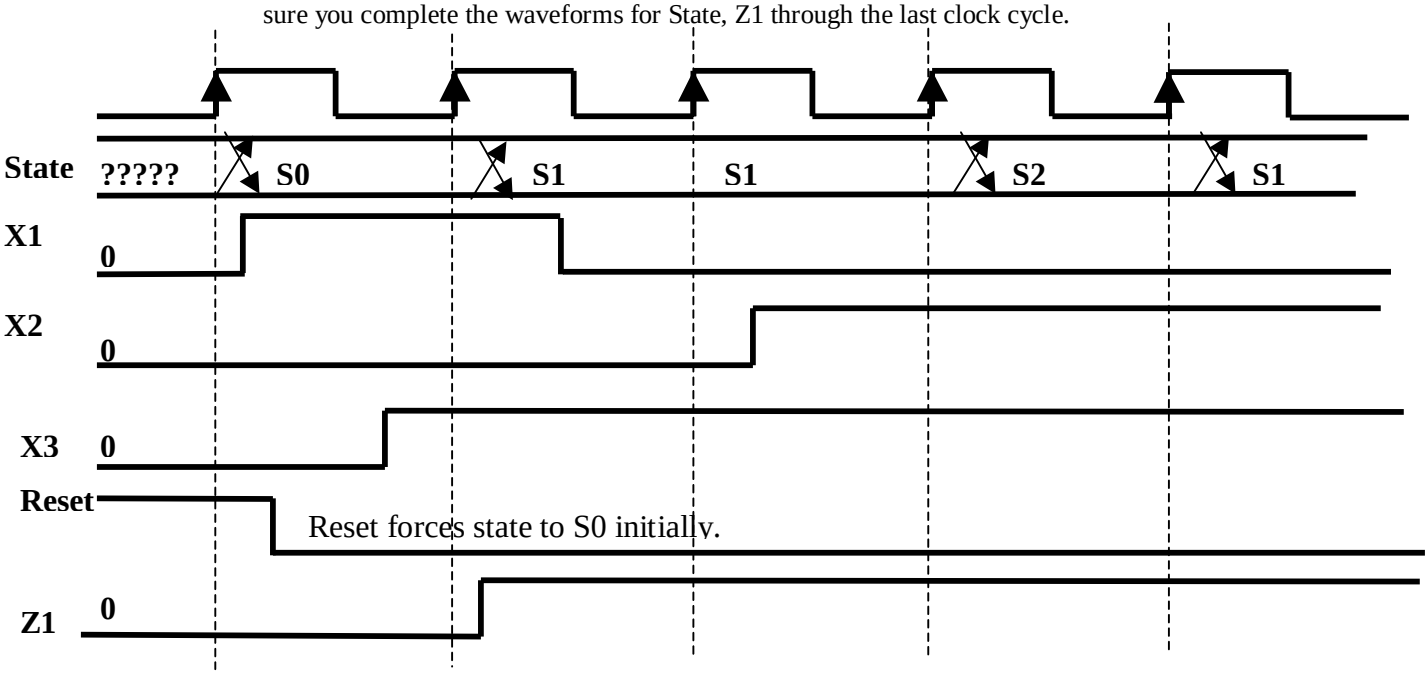
Work all problems.

1. (10 pts) For the ASM chart in Figure #1, the state encoding is one-hot using S0=001, S1=010, S2=100. (see Figure for problem 22.17, pg 586, in book)

   a. Write the boolean equation for the D2 input (D input for state S2 D-Flip-flop)
   D2 = Q2 X2 + Q0 X1' X2 + Q0 X1 X2 X3

   b. Write the boolean equation for the Z1 output.
   Z1 = Q0 X2 + Q1 + Q2

   (15 pts) For the ASM chart in Figure #1, complete the timing diagram below for the State and Z1 waveforms. Assume that rising edge triggered DFFs are used for the FSM implementation. Make sure you complete the waveforms for State, Z1 through the last clock cycle.



2. (10 pts) Refer to the Figure 2 Datapath. Give the value of the counter at the end of state S2 for each of the ASM charts in Figure 2 ASM Charts. You can assume the FSM is in state S0 at the beginning of the timing diagram in Figure 2 Datapath.

   a. ASM Chart a*:* *$46*

   b. ASM Chart *b* *$28*

3. (10 pts).
   Draw a tree network using 2-input AND gates that will perform an AND of 8 inputs (A,B,C,D,E,F,G,H). Give the maximum propagation delay if the delay of each gate is 1 ns.

   See Notes

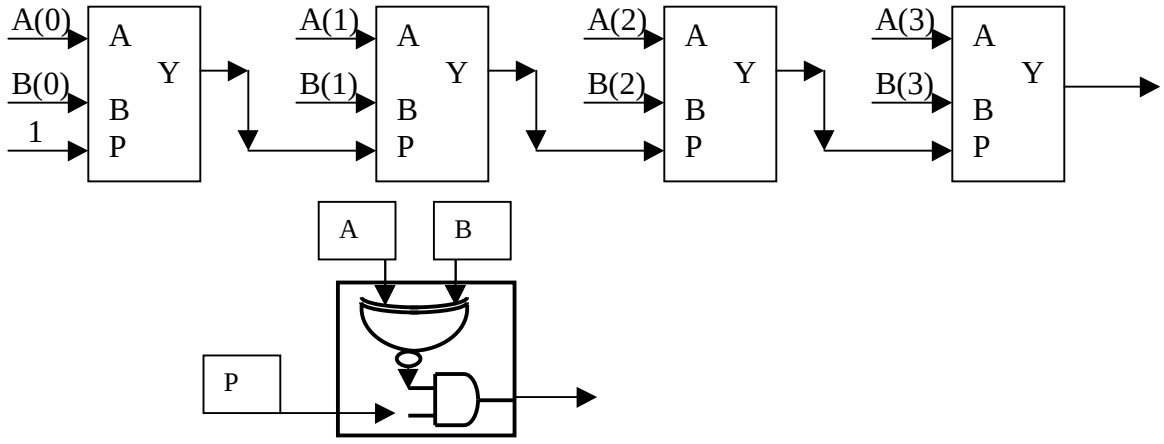
4. (10 pts) Draw the block diagram of an 8-bit adder/subtractor using an 8-bit adder as a building block.

See Notes

5. (10 pts) Draw the ASM chart for a modulo three counter (will count “00”, “01”, “10”, “00”, “01”, ..etc) when EN=1. If EN=0, then the counter will hold its value.

See Notes

6. (10 pts) Below is an iterative network that does equality comparison of two four bit values. Draw the logic that is inside one of the cells (Y <= ‘1’ when (A = B) else ‘0’);



7. (5 pts) Give me a boolean equation that implements the following VHDL statement

Y <= A when (S = ‘0’) else not (B);

Y = A S’ + B’ S’

8. (5 pts) One of the Dice game blocks had an output called “D2312”. This output was true whenever the four bit input SUM was equal to 2, 3, or 12. Give me a boolean equation that implements this.

D2312 <= S3’S2’S1S0 + S3’S2’S1S0 + S3 S2 S1’ S0’

9. (5 pts) Given a 12 state FSM:
   a. How many FFs do I need if I use one-hot encoding? *12*

   b. How many FFs do I need if I use binary count order encoding? *4*

   c. How many FFs do I need if I use Grey code encoding*?* *4*

10. (5 pts) If I have an FPGA that needs to be configured each time it is powered up, what is being used as the primitive logic element*?* *LOOKUP TABLE*

11. (5 pts) What is a requirement for the block that is used as the primitive logic element in an FPGA?

It must be a complete logic family.