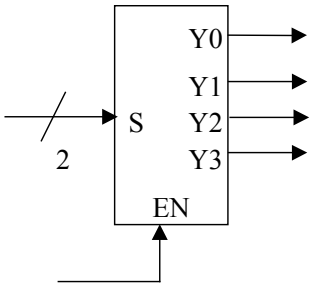
EE 3714 Test #3 - Fall 1999 Solutions

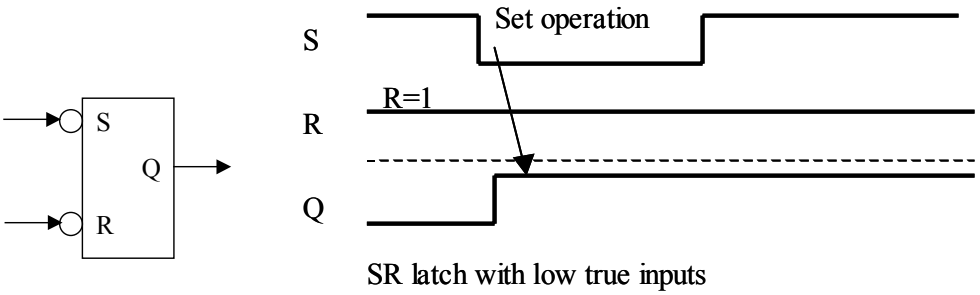
1. (5 pts) Identify the following device. What values do the inputs have to be for the outputs to have the following values Y0= 0, Y1= 0, Y2= 1, Y3=0.



2 to 4 Decoder with Enable

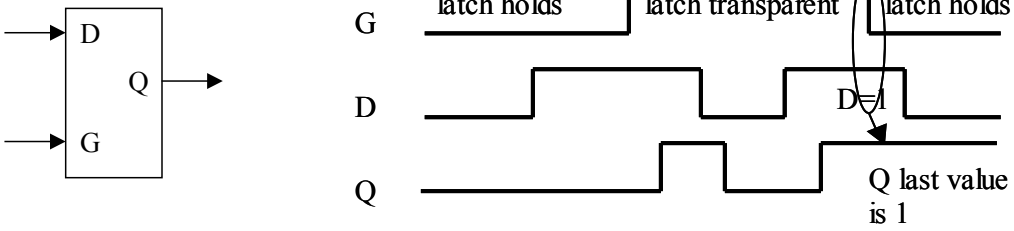
Need S1= 1, S0= 0, EN = 1.

2. (8 pts)Assume that the initial state device shown below is a '0'. Draw a timing diagram that will cause the state of the device to be changed to '1'.

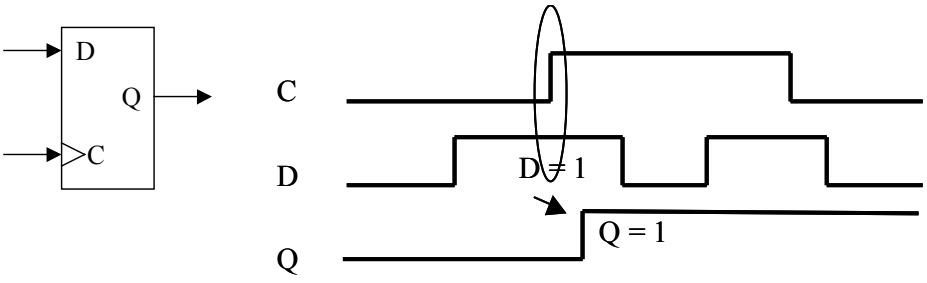


SR latch with low true inputs

3. (8 pts) Complete the timing diagram below for the Q output of the device that is shown.

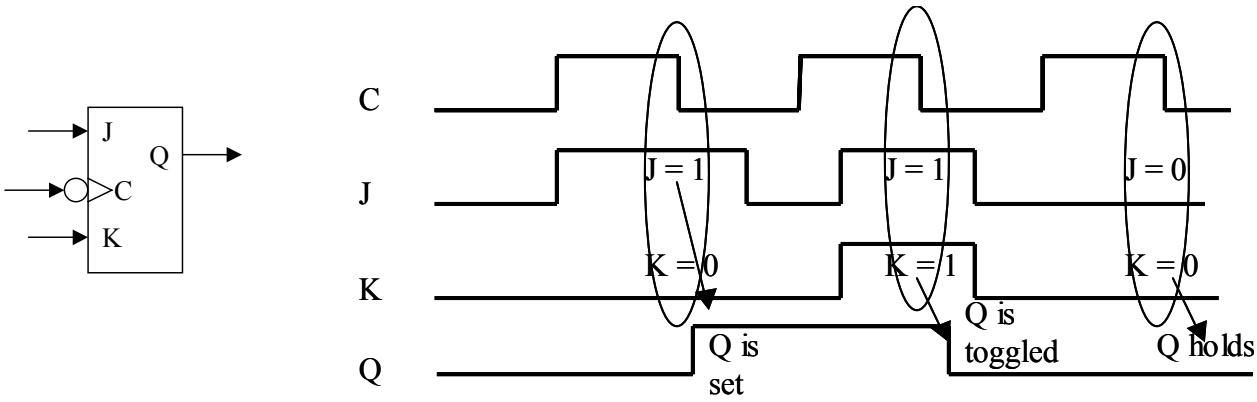


4. (8 pts) Complete the timing diagram below for the Q output of the device that is shown.



Rising edge triggered DFF

5. (8 pts) Complete the timing diagram below for the Q output of the device that is shown.



Falling edge triggered JK.

6. For a flip-flop of your choosing (D, J-K, T) , draw a timing diagram and illustrate setup and hold time constraints. *SEE NOTES ON SETUP/HOLD for DFF*.

7. (5 pts) What is the clock period of a 50 Mhz clock (1 Mhz = 10^6)
   Period = 1/ Frequency = 1/ (50 x $10^{6)}$ = 0.02 x 10^{-6} = 20 x 10^{-9} = 20 ns

8. (5 pts) What is the value of $A3 shifted to the right by one position with the serial input bit = '1'?
   $A3 = 1 0 1 0 0 0 1 1
   Right Shifted value: 1 1 0 1 0 0 0 1 = $D1

9. (5 pts) How is an asynchronous input different from a synchronous input?

Asynchronous inputs are independent of clock, synchronous inputs effect circuit only on active clock edge.

10. Draw the schematic for a 1-bit register. The inputs are CLK, D,LD. The output is Q. The LD input ais high true. *SEE NOTES.*

11. Draw the diagram of a rising edge trigerred D-FF using D Latches. *SEE NOTES (the inverted clock goes to the FIRST D latch, the master latch).*

12. (10 pts) Draw a schematic for a 3- bit counter.… etc.
SEE NOTES.

13. (10 pts) Draw the schematic of a 4-1 mux using Tri-state buffers. You can use an decoder block in your design, and you do not have to show the internal details of the decoder.

SEE NOTES.