9 *N*-bit Adder

This example is “the” verification benchmark circuit. It is useful for demonstrating data abstraction (natural numbers versus bit vectors) and for demonstrating the verification of generic circuits, i.e. circuits with arbitrary bit width.

9.1 Introduction

The circuit computes the sum of two natural number, given as bit vectors of width n. This is probably the most frequently used example in the literature, however, there is a wide variety of restrictions imposed, for example, limitations on n. Is the verification done for arbitrary n? If s is also n-bit what happens at overflow? Furthermore, a variety of realizations are possible ranging from a simple ripple-carry adder to advanced carry lookahead adders.

9.2 Specification

Verify that a realization of an *N*-bit adder computes the sum, *s*, of two n-bit numbers *a* and *b*.

More formally, it is to be shown that

$$\Phi([a_{n-1}, \ldots, a_0]) + \Phi([b_{n-1}, \ldots, b_0]) = \Phi(cout, [s_{n-1}, \ldots, s_0]) \tag{9-1}$$

$$\text{with } \Phi([x_{n-1}, \ldots, x_0]) = \sum_{i=0}^{n-1} 2^i \cdot a_i \tag{9-2}$$

9.3 Implementation

The N-bit adder was designed scalable with step width four. Its four bit components represent carry lookahead structure as described in [Schm78] (Fig. 9-1). It consists of four one bit adders with carry generate and propagate: G_Out = A_In AND B_In P_Out = A_In OR B_In S_Out = C_In XOR (P_Out AND NOT G_Out).

Signals S_Out(i), P_Out(i), G_Out(i) and carry(0) are fed to the carry lookahead generator (Fig. 9-2), which contains a combinational logic to generate B_Propagate, B_Generate, B-Carry and CarryOut(i). The block carry propagate and generate signals may be used to build a real carry lookahead adder with a cascade structure, which is not that easy to build generic.

By connecting the four bit adding units with ripple carry, we now get the complete adder with its inputs DataIn_A, DataIn_B, sum output DataOut and CarryOut (Fig. 9-3). The figure shows an example with 24 bit.

An example simulation is shown in Fig. 9-4.

9.4 Status and Acknowledgments

The circuit has been originally proposed by J. Staunstrup. Most of the actual text is directly quoted from [Stau93]. Thanks to C.-J. Thomas for generating the VHDL descriptions.

9.5 Literature

[Schm78] V. Schmidt. Digitalschaltungen mit Mikroprozessoren. B.G. Teubner Verlag, Stuttgart, 1979. (in german).

[Stau93] J. Staunstrup. IFIP WG 10.2 collection of circuit verification examples, November 1993.

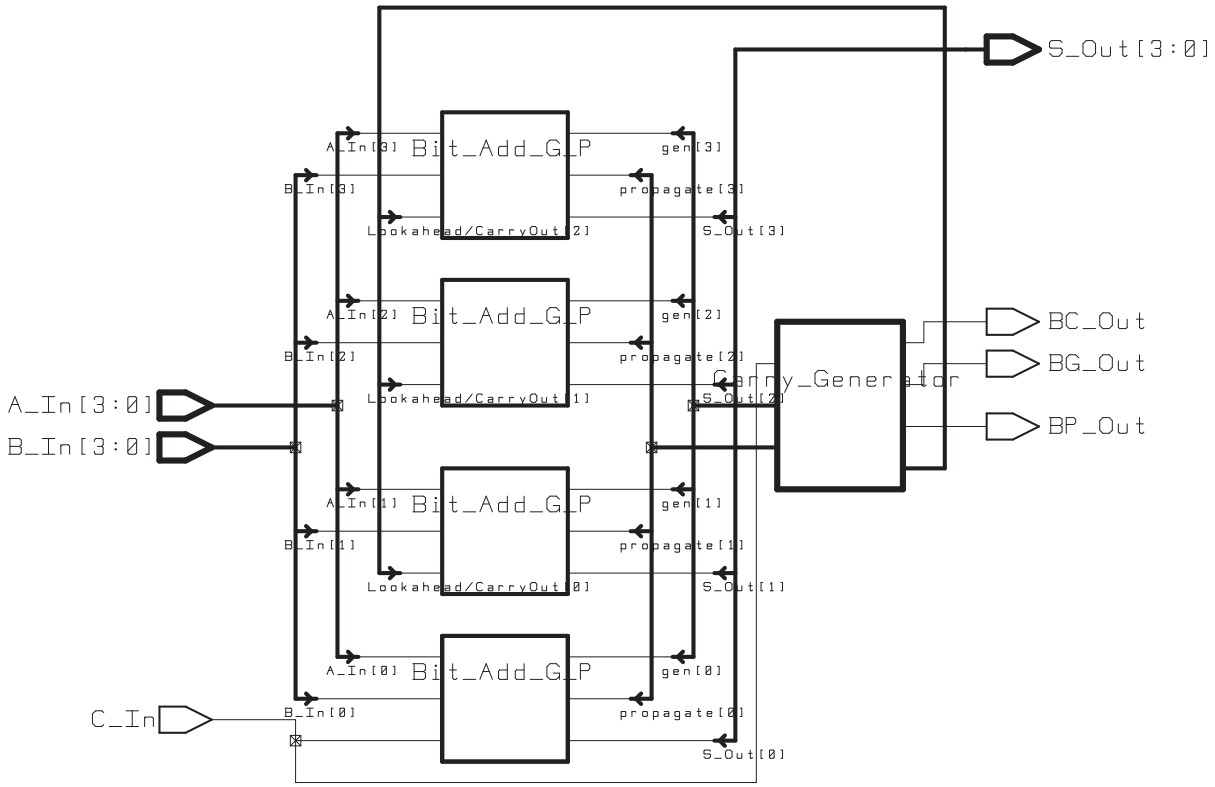

Figure 9-1: 4 bit Base Adder

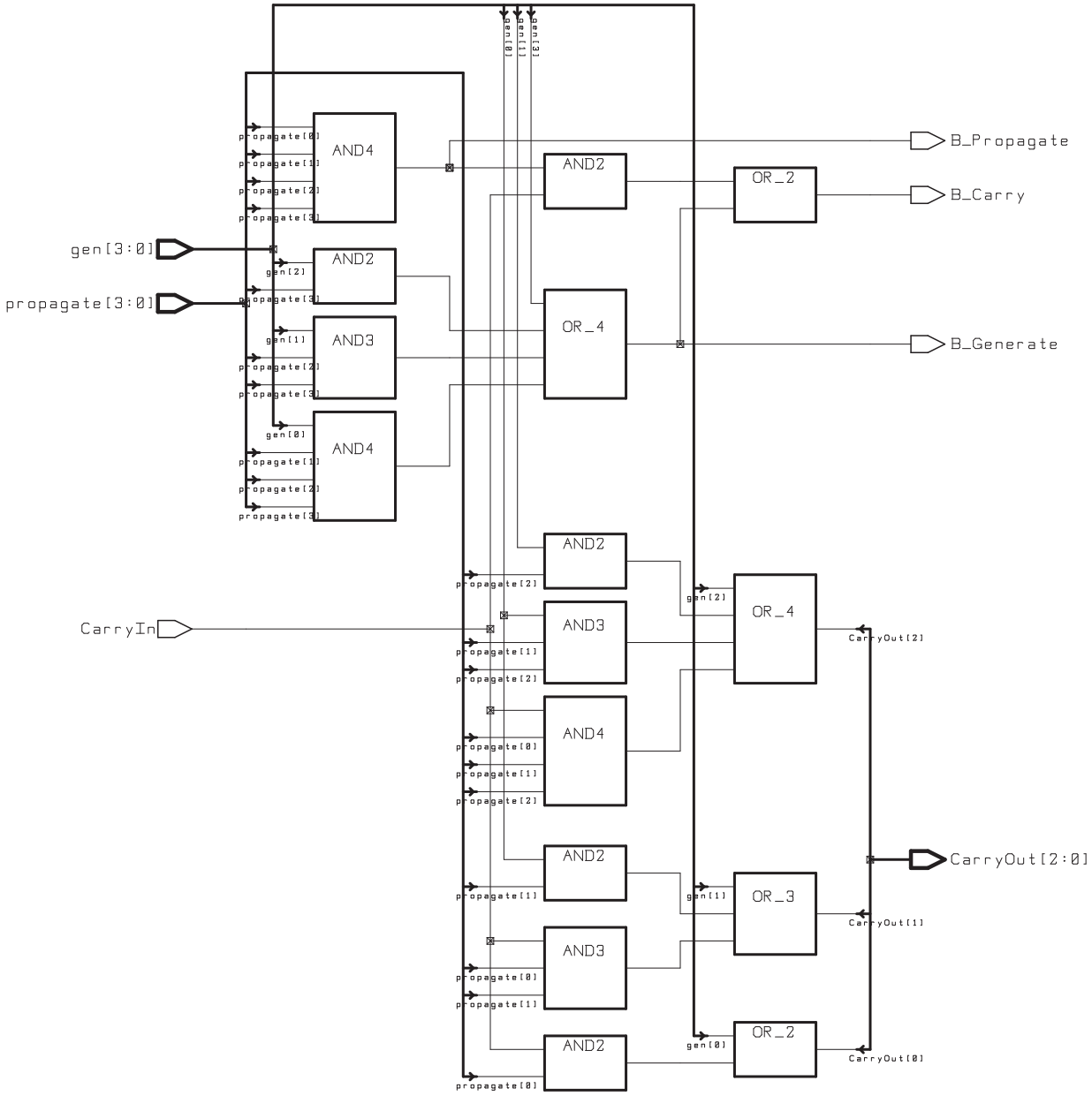

Figure 9-2: Carry Generator

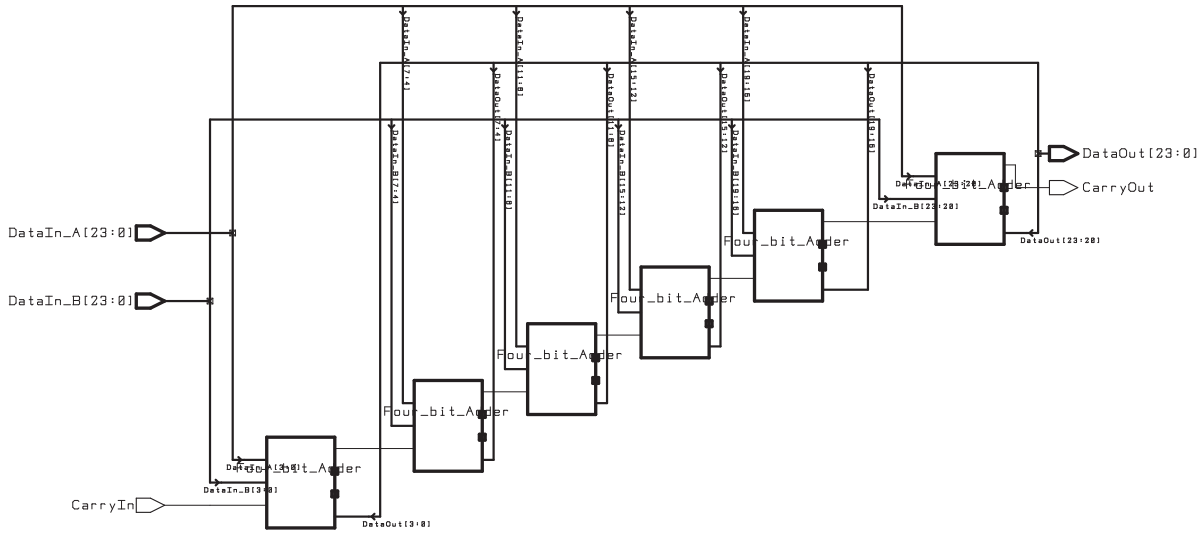

Figure 9-3: 24 Bit Adder

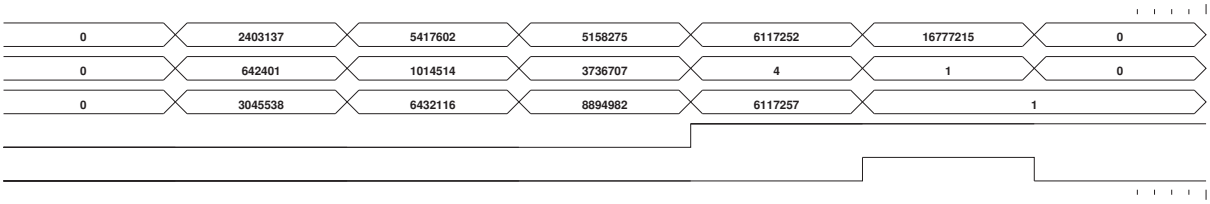

Figure 9-4: Example Simulation