19 FIFO

The FIFO storage element has been chosen, since its implementation is completely asynchronous and does not contain any arithmetic or other computational elements. Thus it is well suited to check verification approaches for their asynchronous capabilities. On the other hand, the circuit is specified in a generic way: it may contain *n* storage elements.

19.1 Specification

The specification of the FIFO element is quite simple and follows the first-in-first-out definition.

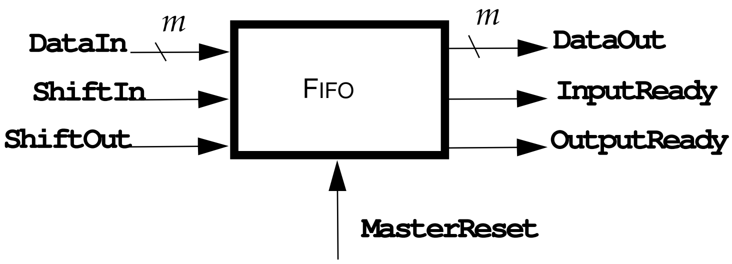

Figure 19-1: Black box view of the FIFO element

Using the input signals given in Fig. 19-1, the following operations should be possible, where “values” denote bit vectors of length *m*:

1. Input a value via **DataIn**, provided that **MasterReset** = 0 and **InputReady** = 1.
2. Output a value via **DataOut**, provided that **MasterReset** = 0 and **OutputReady** = 1.
3. Reset the FIFO element with **MasterReset** = 1.

Hence an overflow of the *n*-place Fifo queue is avoided, if no input is accepted if it is completely filled, i.e. **InputReady** = 0

19.2 Implementation

The implementation is taken from [Schm78]. It is organized using an asynchronous “bubble through” mechanism: input data “fall” automatically to the next free position. It is realized using an asynchronous shift register (Fig. 19-2). Every stage of the shift register consists of a register, i.e. *m* D-flip-flops, responsible for storing the *m* bit vectors. They store data, if a rising edge is applied to their clock signal. Below the shift register cells there is a RS-flip-flop, which indicates, if the respective register contains data (Q =1) or is empty (Q = 0).

Fig. 19-3 and Fig. 19-4 show a realization of one stage and a 4 bit realization, respectively.

Fig. 19-5 shows the simulation of various input and output operations of the FIFO circuit.

19.3 Status and Acknowledgments

Thanks to H.-P. Eich and C.-J. Thomas for designing the circuit in a commercial design system [Fram92].

19.4 Literature

[Schm78] V. Schmidt. *Digitalschaltungen mit Mikroprozessoren*. B.G. Teubner Verlag, Stuttgart, 1979. (in german).

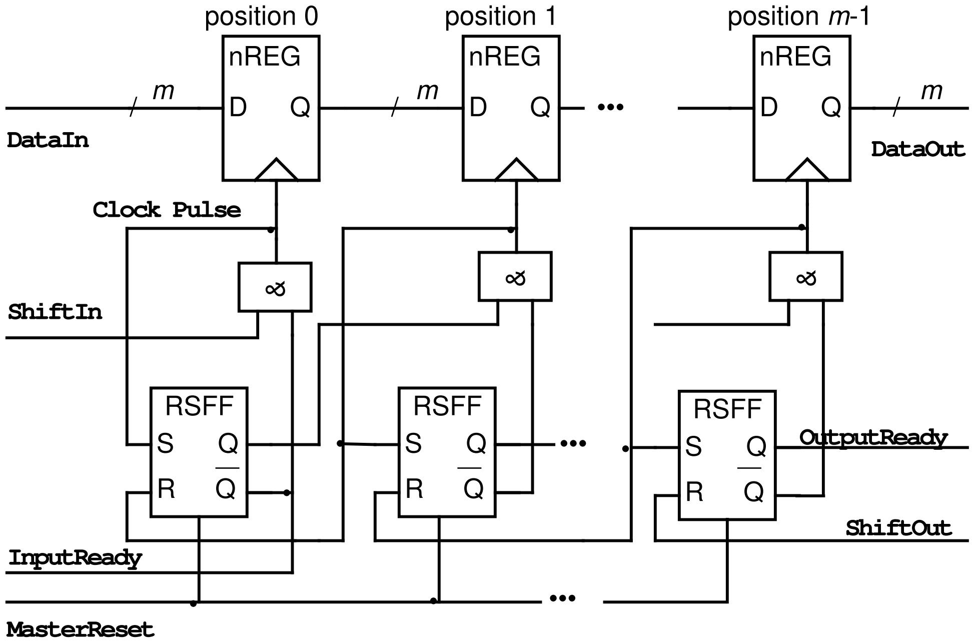

Figure 19-2: Realization of a *m* bit FIFO element with *n* places

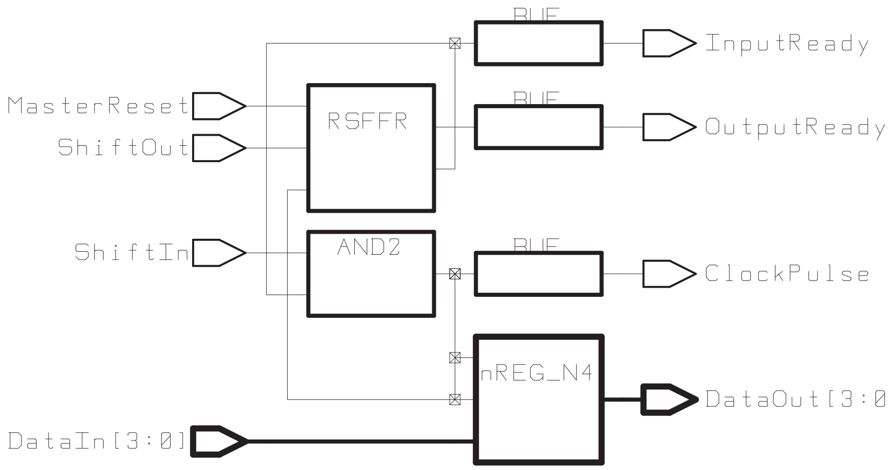

Figure 19-3: Design of one stage of the FIFO element

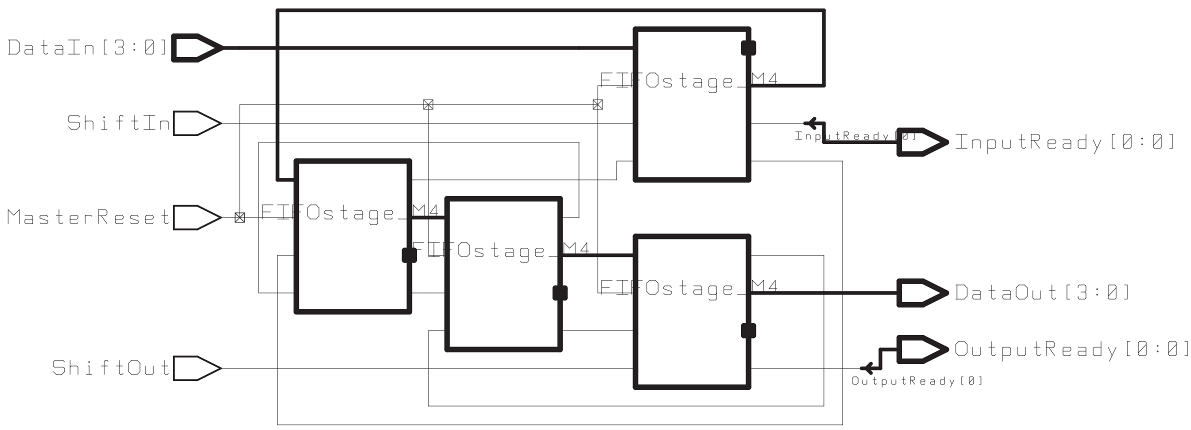

Figure 19-4: Design of a 4-bit FIFO element

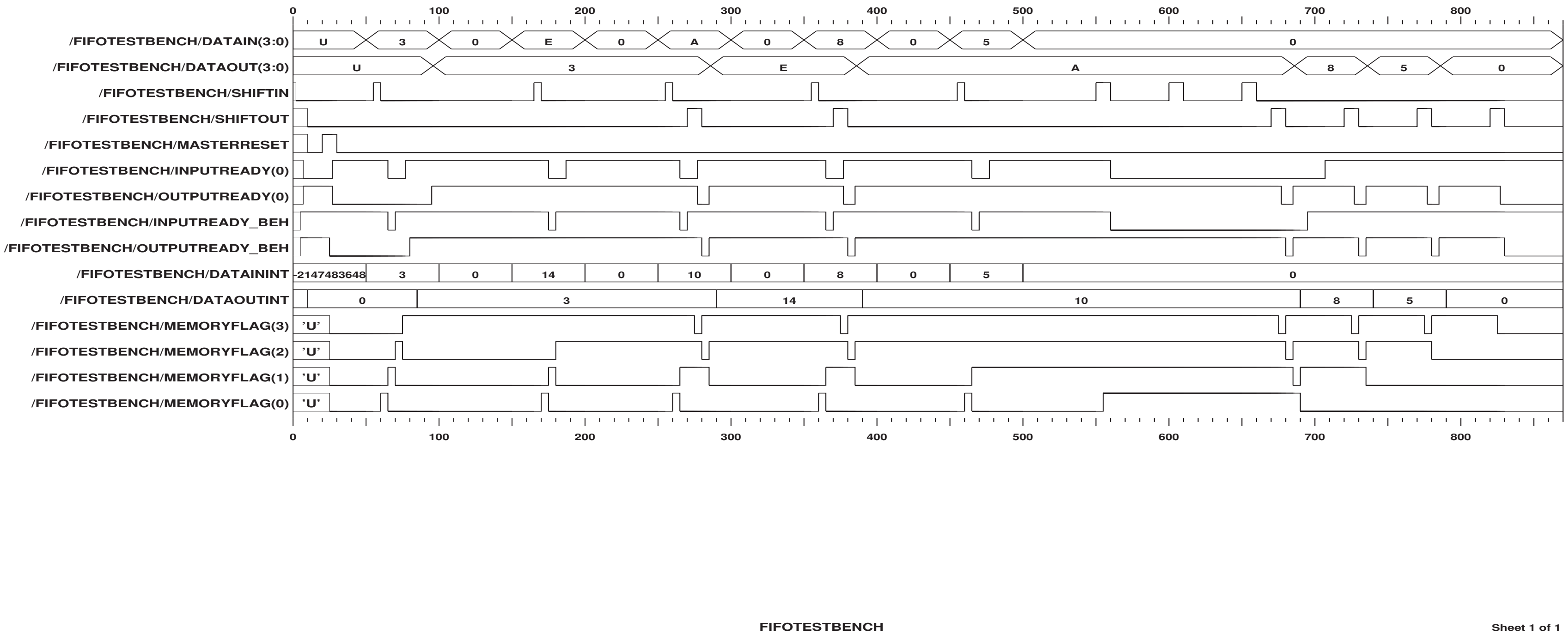

Figure 19-5: Example simulation of the FIFO circuit