Low-Power Logic Styles : CMOS vs CPL

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Abstract

Recently reported logic style comparisons based on full-adder circuits showed complementary pass-transistor logic (CPL) to be much more power efficient than conventional CMOS. New comparisons performed on more efficient CMOS circuit implementations and a wider range of different logic cells and by using realistic circuit arrangements demonstrate CMOS to be superior to CPL in most cases with respect to speed, power dissipation, and power-delay (PT) products.

1 Introduction

The increasing demand for low-power VLSI asks, among others, for power efficient logic styles [1]. Performance criteria for logic styles are circuit speed, circuit size, power dissipation, and wiring complexity as well as ease-of-use and generality of gates in cell-based design techniques. Dynamic logic styles are often a good choice for high-speed, but not for low-power circuit implementations due to the high node activity and large clock loads [1]. This paper focuses on static logic styles suitable for low-power implementation of arbitrary combinational circuits.

2 Static Logic Styles

Conventional CMOS, in combination with *pass-gate logic*, allows very efficient implementation of simple gates (e.g. NAND/NOR, AOI/OAI) having only few transistors and nodes, and a small delay due to the single inversion level. The disadvantages lie in the large PMOS transistors resulting in high input capacitances and area requirements, and the weak output driving capability caused by series transistors.

Complementary pass-transistor logic (CPL) [1] benefits from the small input capacitances (NMOS network only), the fast differential stage, and the good output driving capability (output inverter), making the implementation of complex gates (e.g. full-adders) very efficient. On the other hand, the large number of nodes and transistors and the two inversion levels result in relatively inefficient CPL implementations of simple gates. Usually, pull-up PMOS transistors are necessary for swing restoration. Larger short-circuit currents and higher wiring overhead (dual-rail signals) compared to CMOS also increase power consumption.

Swing restored pass-transistor logic (SRPL) [2] and *double pass-transistor logic* (DPL) [3] are closely related to CPL and are also considered in the subsequent comparisons.

3 Comparisons and Results

3.1 Simple and Complex Gates

The first set of comparisons was done on various simple and complex gates under realistic circuit arrangements and simulation conditions. Circuits were designed at the transistor-level in a standard 0.6μm process technology and simulated using Hspice at 3.3V, 27°C, and estimated diffusion and wiring capacitances. Transistors were sized carefully by hand with the objective of minimal PT-product. Some of the circuits are depicted in Fig. 1 with the transistor sizes given in λ (λ = 0.3μm).

Fig. 2 shows the general circuit set-up used for simulation. Several gates of the same type are connected in series with typical interconnect loads (50fF) attached and a fan-out of two except for the full-adders, where a fan-out of one is realistic (e.g. adder array, Wallace tree). This set-up makes sure that all inputs are driven by typical gate outputs and not by the simulator, which makes a significant difference especially for pass-transistor and pass-gate circuits. In these logic styles in particular, a signal may fan-out to both a transistor gate and a transistor source at the same time. The current drawn by the source thereby slows down the signal ramp and thus the switching of the transistor driven by the gate. These effects are taken into account by simulating various possible input combinations into the two subsequent gates a gate output fans out (Fig. 2).

Most logic style comparisons reported in the literature base on the full-adder circuit (FA) and an inefficient CMOS version (40 transistors). Its 3-input XOR function is perfectly suited for CPL, resulting in the fastest possible implementation. However, the CMOS implementation from Fig. 1a (28 transistors) consumes much less power, and its PT-product is larger by only 10% compared to CPL. DPL is not competitive at all with respect to area, delay, and power due to the very high transistor count. All comparison numbers are summarized in Table 1. Note that power and delay can be traded off by a considerable amount for each gate using transistor sizing, and that the numbers here are given for the solutions with the smallest PT-product.

Additionally, the following gates were compared: 2-input NAND (NAND2), 4-input AND (AND4), 3-input and-or-invert/or-and-invert (AOI/OAI), 2- and 4-input multiplexer (MUX2/ MUX4), and 2-input XOR. Here, CMOS clearly outperforms CPL with respect to power dissipation, power-delay product, number of transistors, and – in most cases – even circuit delay. The bad performance numbers for the SRPL AOI-gate document the weak driving capability of SRPL and the fact that gates implemented in this logic style cannot be connected in series to form arbitrary circuits.

Table 1: Gate comparisons.

cell type	logic style	delay (ns)	power (μW)	PT (norm.)	# trans.	cell type	logic style	delay (ns)	power (μW)	PT (norm.)	# trans.
FA	CMOS	1.94	65	1.00	28	AOI/OAI	CMOS	1.17	41	1.00	6
	CMOS [1]	1.96	78	1.20	40		CPL	1.12	80	1.89	14
	TGATE [2]	1.85	82	1.20	24		SRPL	4.48	108	10.21	12
	CPL	1.17	97	0.90	32	MUX2	CMOS	0.93	46	1.00	8
	DPL	2.03	119	1.91	48		CPL	1.24	57	1.66	10
	WANG [3]	1.68	81	1.08	25	MUX4	CMOS	1.39	62	1.00	18
NAND2	CMOS	0.67	37	1.00	4		CPL	1.55	66	1.19	18
	CPL	1.17	65	3.09	10	XOR2	CMOS	1.27	38	1.00	8
AND4	CMOS	1.09	44	1.00	12		CPL	1.29	59	1.58	10
	CPL	1.48	98	3.02	18		WANG [3]	1.27	51	1.33	6

[1] CMOS version used in most comparisons [1]
[3] XOR proposed by Wang [5]
[2] Pure transmission-gate version

3.2 32-Bit Adder

A 32-bit adder was realized in a 0.5μm CMOS process using the unbounded fan-out buffered parallel-prefix adder structure of Fig. 3 [4]. It was simulated at 2.8V, 110°C, and 100MHz with estimated parasitic capacitances. The CMOS implementation makes use of the efficient AOI/OAI-gates, while the CPL solution realizes the carry-propagation with multiplexers. Table 2 gives the comparison results. The CMOS solution is about 20% slower than the CPL version, but has a much smaller transistor count and consumes less than 1/3 of the power.

4 Conclusions

The advantages of high functionality with few pass-transistors and of small input capacitances in the CPL style are partially undone by the need for swing restoration circuitry, dual-rail encoding, and the resulting wiring overhead, which becomes a crucial factor in deep submicron. The presented investigation results show that – for most simple and complex logic gates and under realistic circuit conditions – conventional CMOS combined with pass-gate logic performs much better than CPL and related logic styles if low power is concerned.

References

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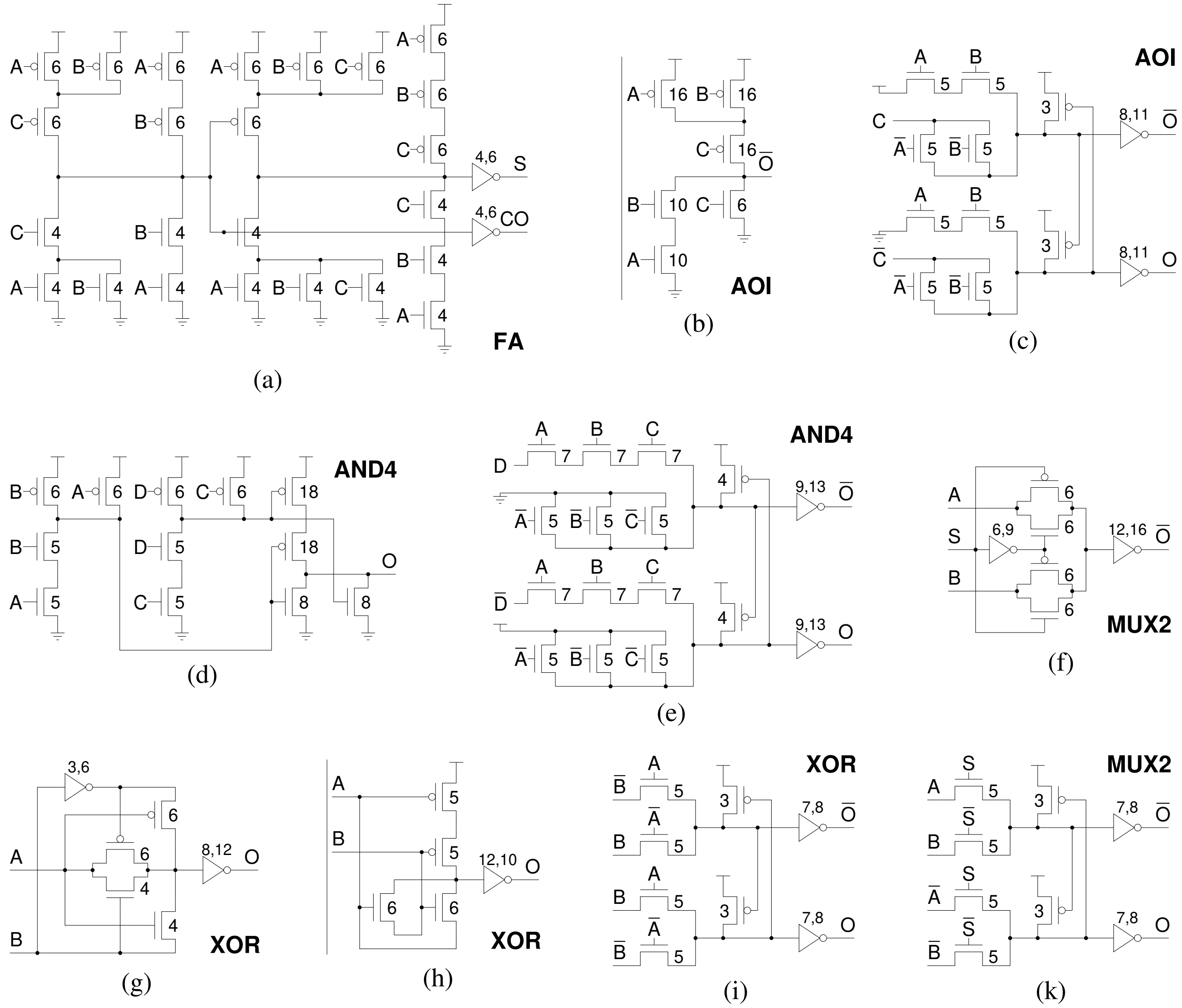

Fig. 1: (a, b, d, f, g) CMOS gates, (c, e, i, k) CPL gates, and (h) Wang's XOR.

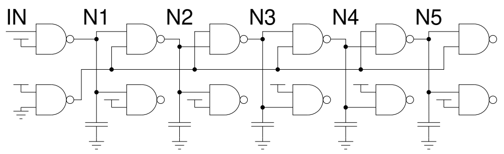

Fig. 2: Circuit set-up for simulation.

Table 2: 32-bit adder comparisons.

logic style	delay (ns)	power (mW)	PT (norm.)	# trans.
CMOS	4.14	7.50	1.00	1607
CPL	3.47	25.90	2.89	2774
CPL [4]	4.73	16.80	2.56	2774

[4] down-sized transistors

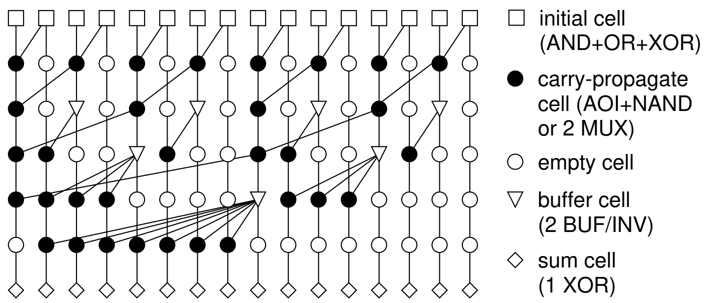

Fig. 3: Buffered parallel-prefix adder structure.