Comment on new differential flipflops from Yuan and Svensson

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ABSTRACT

A family of differential latches has recently been proposed by Yuan and Svensson[1]. In this letter we show that the proposed flipflops using the dynamic slave latch suffer from a poor logic-level zero in the presence of glitches on the data inputs.

I. Introduction

In a recent paper, Yuan and Svensson [1] proposed new differential latches, as shown in figure 1, and flipflops formed by pairs of master and slave latches. The operation of the flipflops is as follows. When the clock is low, the slave latch holds its output and the new value is established on the outputs of the master; these form the inputs to the slave and when the clock goes high, the slave switches accordingly. The key point is that while the clock remains high, the outputs of the master latch either hold their value or the one which is high discharges to Gnd; thus, since they are connected to the slave through n-type transistors, the master outputs cannot switch the slave to another value.

In this letter we show that flipflops formed using the dynamic slave latch suffers from a poor logic-level zero in the presence of glitches on the data inputs.

II. Problem with input glitches

We consider the flipflop formed from the two dynamic latches in figure 1 and highlight a problem associated with input glitches. The problem lies with the dynamic slave latch and the following discussion would also apply to a flipflop formed from the static master and the dynamic slave latches.

The flipflop has differential inputs. We consider the case of glitches when both the x and $\bar{x}$ switch together and then return to their original values. Figure 2 shows an HSPICE simulation of the flipflop formed from the two dynamic latches with all transistor sizes equal to W=2u and L=0.8u, and using ES2-Atmel's ECPD07 CMOS technology.

The input *in* is driven at 0V during both the rising and falling clock edges but glitches to 5V during both phases of the clock. The latch is initialized to *out* = high; and on the first rising clock edge, the outputs *out* and $\overline{out}$ switch to low and high respectively corresponding to the values in *in* and $\overline{in}$.

During the low clock phase, the *out* node shows two deviations from Gnd which could cause static power dissipation in the next logic stage thus making the dynamic slave latch unsuitable for low-power applications. The two deviations relate to two different and independent mechanisms, both associated with glitches in the flipflop inputs.

The first deviation from Gnd is due to the coupling capacitance of the gate between nodes x and *out*. Due to the first glitch (during the clock-high phase), both outputs of the master latch (x and $\bar{x}$) are discharged. When the clock becomes low, *out* becomes isolated and x rises as the master is reconnected to the power source: the cross-coupling between x and *out* causes *out* to rise.

The second deviation from Gnd is due to charge sharing between nodes x and bj. When the clock becomes low, the node bj is isolated but discharged. When, due to the second glitch (during the clock-low phase), $\bar{x}$ rises (i.e. x falls) the node bj is connected to $\overline{out}$ which is itself connected to the power supply; thus bj charges up to $(Vdd - V_{Tn})$. When x then rises (i.e. $\bar{x}$ falls) the node bj is disconnected from $\overline{out}$ and connected to out, and the charge on bj is shared between bj and out causing out to rise.

III. Conclusion

In considering the new differential latches[1] of Yuan and Svensson, we have shown that flipflops which include the dynamic slave latch have a problem whereby input glitches during either phase of the clock lead to a poor logic-level zero on the outputs by two independent mechanisms. This behaviour makes the dynamic slave latch unsuitable as part of a flip-flop design for low-power applications.

References

1. J Yuan and C Svensson, ‘‘New TSPC latches and flipflops minimizing delay and power’’, *Symposium on VLSI Circuits Digest of Technical Papers*, pp. 160-161, 1996.

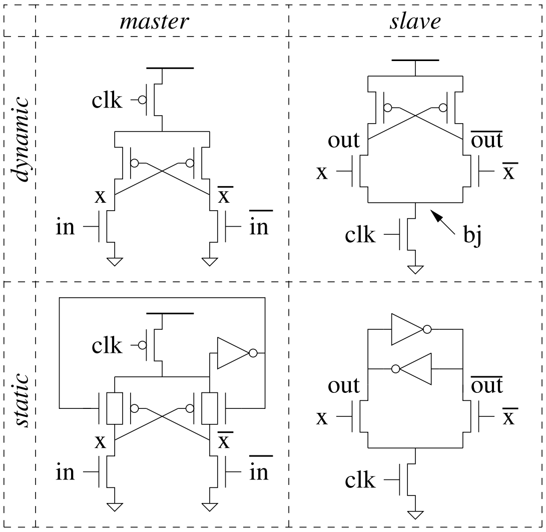

Figure 1. Yuan and Svensson differential latches[1]

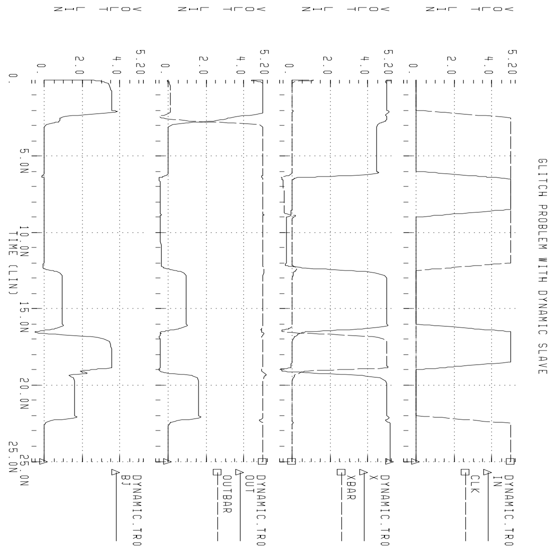

Figure 2. HSPICE showing glitch problem